Response Under 37 C.F.R. § 1.116 - Expedited Procedure
Examining Group 2814

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re the application of: Anthony *et al.*		Docket:	TI-24953
Appl. No.:	**09/116,138**	Examiner:	**A. Mai**
Filed:	07/15/98	Art Unit:	**2814**
For:	High Permittivity Silicate Gate Dielectric		

AMENDMENT PURSUANT TO 37 C.F.R. § 1.116

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on April 15, 2002.

David Denker Reg. No. 40,987

February 7, 2002

Ass't Commissioner for Patents
Washington, DC 20231

Examiner:

In response to the Office Action dated January 14, 2002, please amend the patent application as follows.

IN THE SPECIFICATION

A. Page 7, please add the following paragraphs at the bottom.

-- Figs. 19-20 are cross-sectional views of a semiconductor device during fabrication according to a fifth preferred embodiment of the invention.

Fig. 21 is a simplified cross-sectional view of a field effect transistor using the current invention.--

B. Page 18, please add the following paragraph after line 2.

-- Fig. 21 shows a simplified view of a completed transistor. Semiconductor substrate 100 has a channel region 120. Channel 120 is disposed between source 140 and drain 160. Conductive gate 38 overlies silicate gate dielectric 36.--

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